Appl. No. 10/669,515
Amdt. dated 05/02/05
Reply to Office Action of 03/08/05

Attorney Docket No.: N1280-04900
TSMC 2002-1091

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1   1.   (Currently Amended)   A method to reduce switching noise on an integrated
2   circuit device, said method comprising:
3   providing an integrated circuit device comprising an upper voltage node, a
4   ground, and a plurality of switchable capacitors wherein each said switchable capacitor
5   is connected from said upper voltage node to said ground;
6   tracking an operating mode of said integrated circuit device;
7   selecting an optimal capacitance value based on said operating mode <u>by</u>
8   <u>determining a proportion of total circuits in said integrated circuit device that are</u>
9   <u>switching in said operating mode and calculating said optimal capacitance value based</u>
10   <u>on said proportion</u>; and
11   selecting a set of said switchable capacitors from said plurality of switchable
12   capacitors to thereby connect said optimal capacitance value from said upper voltage
13   node to said ground.

1   2.   (Cancelled)

1   3.   (Currently Amended)   The method according to Claim [[2]] <u>1</u> wherein said
2   optimal capacitance value is calculated using a formula based on capacitance loading in
3   switching circuits and capacitance loading in non-switching circuits.

1   4.   (Original)   The method according to Claim 1 wherein said operating mode
2   comprises a power-saving mode.

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1 5.   (Original)   The method according to Claim 1 wherein said switchable
2 capacitors each comprise a capacitor and a switch connected in series.

1 6.   (Original)   The method according to Claim 5 wherein said capacitor comprises
2 an MOS device.

1 7.   (Original)   The method according to Claim 5 wherein said capacitor is
2 connected to said upper voltage node and said switch is connected to said ground.

1 8.   (Original)   The method according to Claim 5 wherein said capacitor is
2 connected to said ground and said switch is connected to said upper voltage node.

1 9.   (Original)   The method according to Claim 5 wherein said switch comprises an
2 MOS transistor.

1 10.   (Original)   The method according to Claim 1 wherein said switchable
2 capacitors each comprise:
3   a PMOS transistor having source, drain, and gate terminals wherein said source
4 terminal is coupled to said upper voltage node;
5   an NMOS transistor having source, drain, and gate terminals wherein said
6 source terminal is coupled to said ground, wherein said drain terminal is coupled to said
7 PMOS transistor gate terminal, and wherein said gate terminal is coupled to said PMOS
8 transistor drain terminal;
9   a first switch coupled between said PMOS transistor gate terminal and said
10 upper voltage node; and
11   a second switch coupled between said NMOS transistor gate terminal and said
12 ground.

1 11.   (Original).   The method according to Claim 10 wherein said first and second
2 switches comprise MOS transistors.

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1   12.   (Original)   A method to reduce switching noise on an integrated circuit device,
2   said method comprising:
3   providing an integrated circuit device comprising an upper voltage node, a
4   ground, and a plurality of switchable capacitors wherein each said switchable capacitor
5   is connected from said upper voltage node to said ground and wherein said switchable
6   capacitors each comprise a capacitor and a switch connected in series;
7   tracking the operating mode of said integrated circuit device;
8   selecting an optimal capacitance value based on said operating mode by a
9   method comprising:
10   determining a proportion of total circuits in said integrated circuit device that are
11   switching in said operating mode; and
12   calculating said optimal capacitance value based on said proportion; and
13   selecting a set of said switchable capacitors from said plurality of switchable
14   capacitors to thereby connect said optimal capacitance value from said upper voltage
15   node to said ground.

1   13.   (Original)   The method according to Claim 12 wherein said optimal
2   capacitance value is calculated using a formula based on capacitance loading in
3   switching circuits and capacitance loading in non-switching circuits.

1   14.   (Original)   The method according to Claim 12 wherein said operating mode
2   comprises a power-saving mode.

1   15.   (Original)   The method according to Claim 12 wherein said capacitor
2   comprises an MOS device.

1   16.   (Original)   The method according to Claim 12 wherein said capacitor is
2   connected to said upper voltage node and said switch is connected to said ground.

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1   17.   (Original)   The method according to Claim 12 wherein said capacitor is

2   connected to said ground and said switch is connected to said upper voltage node.

1   18.   (Original)   The method according to Claim 12 wherein said switch comprises

2   an MOS transistor.

1   19.   (Previously Presented)   An integrated circuit device comprising:

2   an upper voltage node;

3   a ground;

4   a plurality of switchable capacitors wherein each said switchable capacitor is

5   connected from said upper voltage node to said ground;

6   means for tracking the operating mode of said integrated circuit device;

7   means for selecting an optimal capacitance value based on said operating mode;

8   and

9   means for selecting a set of said switchable capacitors from said plurality of

10   switchable capacitors to thereby connect said optimal capacitance value from said

11   upper voltage node to said ground.

1   20.   (Previously Presented)   The device according to Claim 19 wherein said

2   means of selecting an optimal capacitance value based on said operating mode

3   comprises:

4   means for determining a proportion of total circuits in said integrated circuit

5   device that are switching in said operating mode; and

6   \ means for calculating said optimal capacitance value based on said proportion.

1   21.   (Original)   The device according to Claim 20 wherein said optimal capacitance

2   value is calculated using a formula based on capacitance loading in switching circuits

3   and capacitance loading in non-switching circuits.

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1 22. (Original) The device according to Claim 19 wherein said operating mode
2 comprises a power-saving mode.

1 23. (Original) The device according to Claim 19 wherein said switchable
2 capacitors each comprise a capacitor and a switch connected in series.

1 24. (Original) The device according to Claim 23 wherein said capacitor comprises
2 an MOS device.

1 25. (Original) The device according to Claim 23 wherein said capacitor is
2 connected to said upper voltage node and said switch is connected to said ground.

1 26. (Original) The device according to Claim 23 wherein said capacitor is
2 connected to said ground and said switch is connected to said upper voltage node.

1 27. (Original) The device according to Claim 23 wherein said switch comprises
2 an MOS transistor.

1 28. (Original) The device according to Claim 19 wherein said switchable
2 capacitors each comprise:
3   a PMOS transistor having source, drain, and gate terminals wherein said source
4 terminal is coupled to said upper voltage node;
5   an NMOS transistor having source, drain, and gate terminals wherein said
6 source terminal is coupled to said ground, wherein said drain terminal is coupled to said
7 PMOS transistor gate terminal, and wherein said gate terminal is coupled to said PMOS
8 transistor drain terminal;
9   a first switch coupled between said PMOS transistor gate terminal and said
10 upper voltage node; and
11   a second switch coupled between said NMOS transistor gate terminal and said
12 ground.

1   29.   (Original)   The device according to Claim 28 wherein said first and second
2   switches comprise MOS transistors.

1   30.   (Original)   The device according to Claim 28 wherein said first and second
2   switches are controlled by a single signal.

1   31.   (Previously Presented) A method to reduce switching noise on an integrated
2   circuit device, said method comprising:
3   providing an integrated circuit device comprising an upper voltage node, a
4   ground, and a plurality of switchable capacitors wherein each said switchable capacitor
5   is connected from said upper voltage node to said ground;
6   tracking an operating mode of said integrated circuit device;
7   selecting an optimal capacitance value based on said operating mode by
8   determining a proportion of total circuits in said integrated circuit device that are
9   switching in said operating mode and calculating said optimal capacitance value based
10   on said proportion; and
11   selecting a set of said switchable capacitors from said plurality of switchable
12   capacitors to thereby connect said optimal capacitance value from said upper voltage
13   node to said ground.

1   32.   (Previously Presented) An integrated circuit device comprising:
2   an upper voltage node;
3   a ground;
4   a plurality of switchable capacitors wherein each said switchable capacitor is
5   connected from said upper voltage node to said ground;
6   means for tracking the operating mode of said integrated circuit device;
7   means for selecting an optimal capacitance value based on said operating mode;
8   and
9   means for selecting a set of said switchable capacitors from said plurality of
10   switchable capacitors to thereby connect said optimal capacitance value from said

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11 upper voltage node to said ground, wherein said means of selecting an optimal

12 capacitance value based on said operating mode comprises:

13   means for determining a proportion of total circuits in said integrated circuit

14 device that are switching in said operating mode; and

15   means for calculating said optimal capacitance value based on said proportion.